CS315-02 Processor Design Components

Project 05 ⇒ incremental development

C coding
Data representation
Memory
RISC-V Assembly
RISC-V Machine Code
RISC-V Emulator
Cache Design
Digital Design

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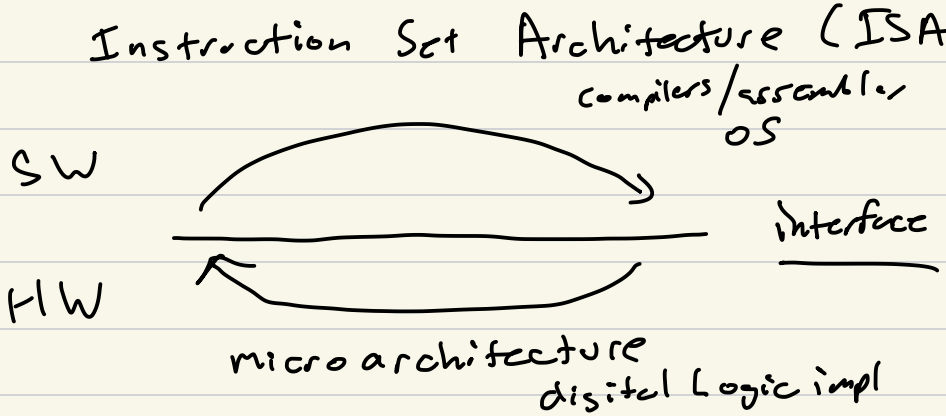
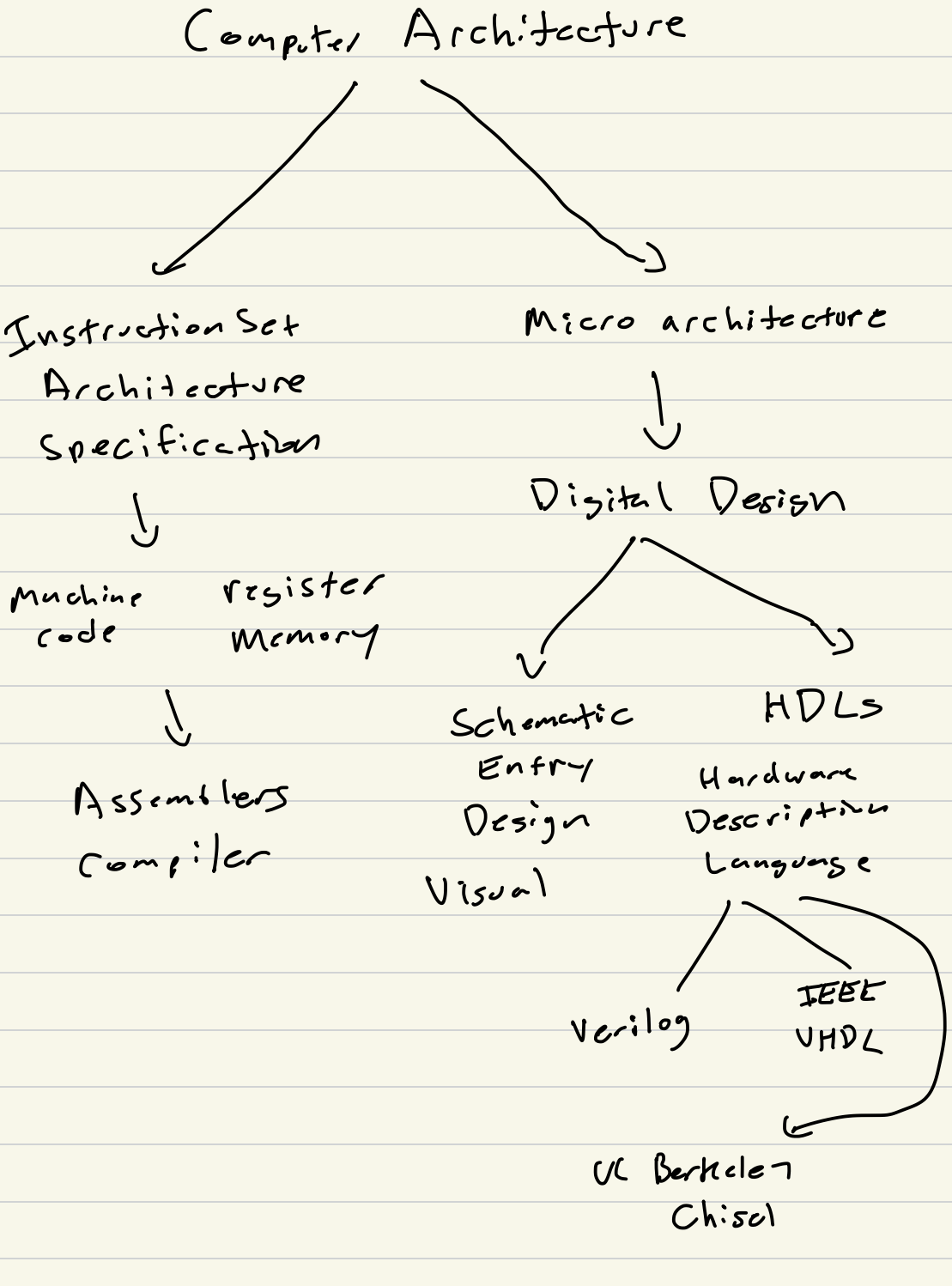
Processor Design




Computer Architecture
Instruction Set Architecture Specification
Machine code
register Memory
Assemblers Compiler
Micro architecture
Digital Design
Schematic Entry Design
Visual
HDLs
Hardware Description Language
Verilog
IEEE VHDL
UC Berkeley Chisel

Processor Design

Moore's Law

The number of transistors doubles every 1.5 years.

increase size
increase density

Two micro architectures

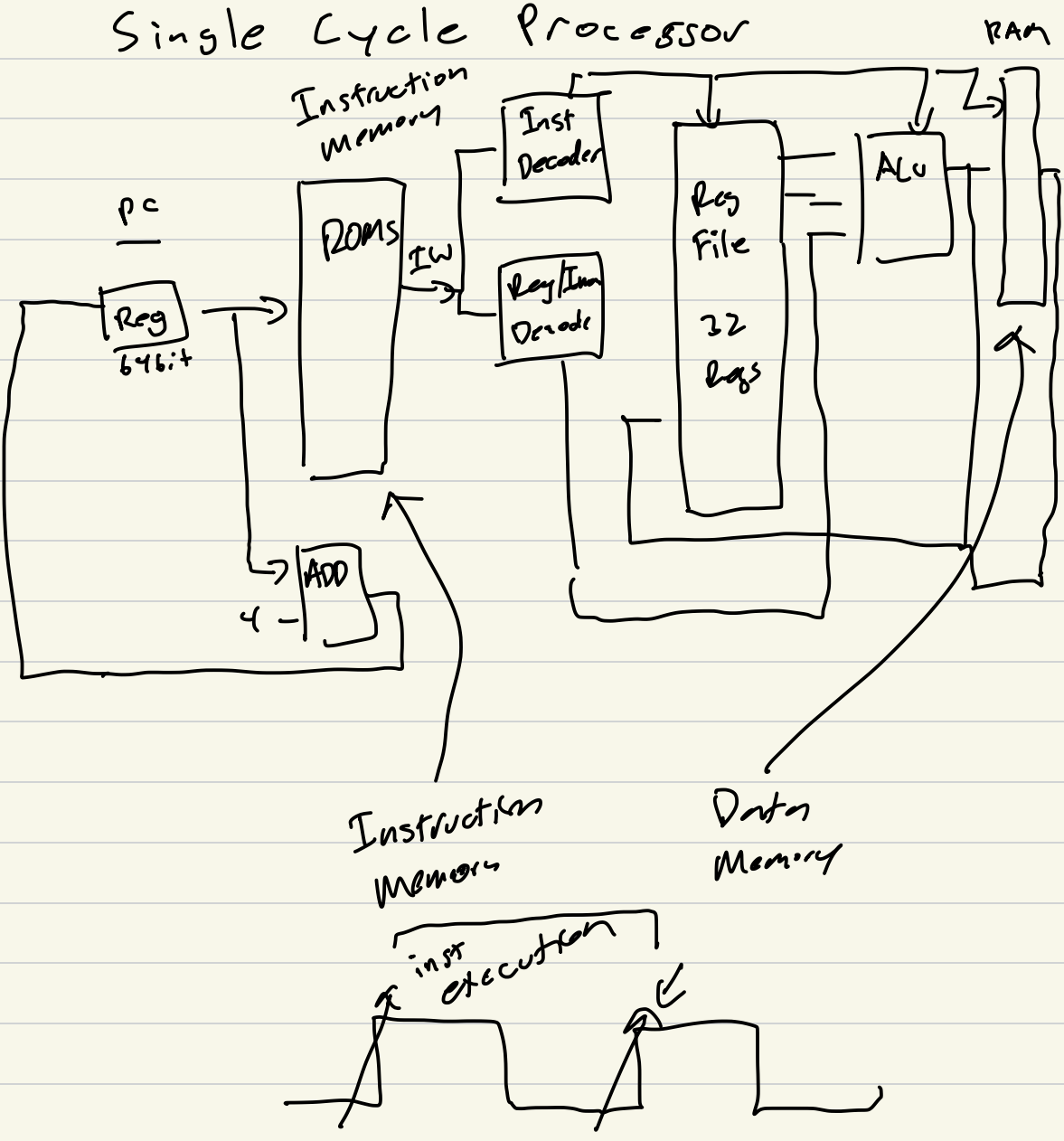
single-cycle processor
[multi-cycle]
pipelined processor

} this class

super scalar
out-of-order execution
speculative execution

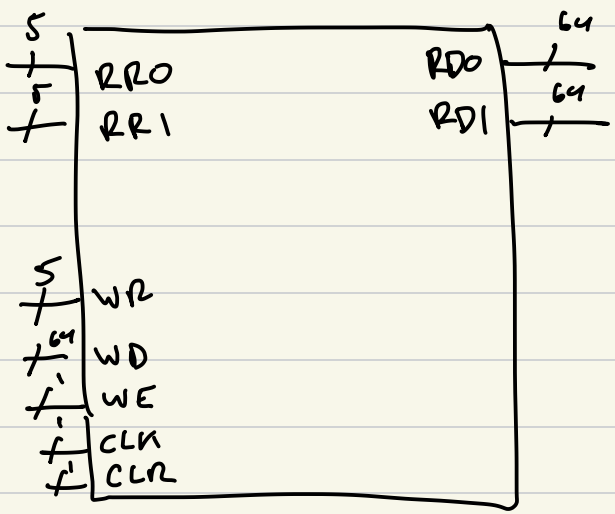
Lab05 → Lab06 → Project06

Single Cycle Processor



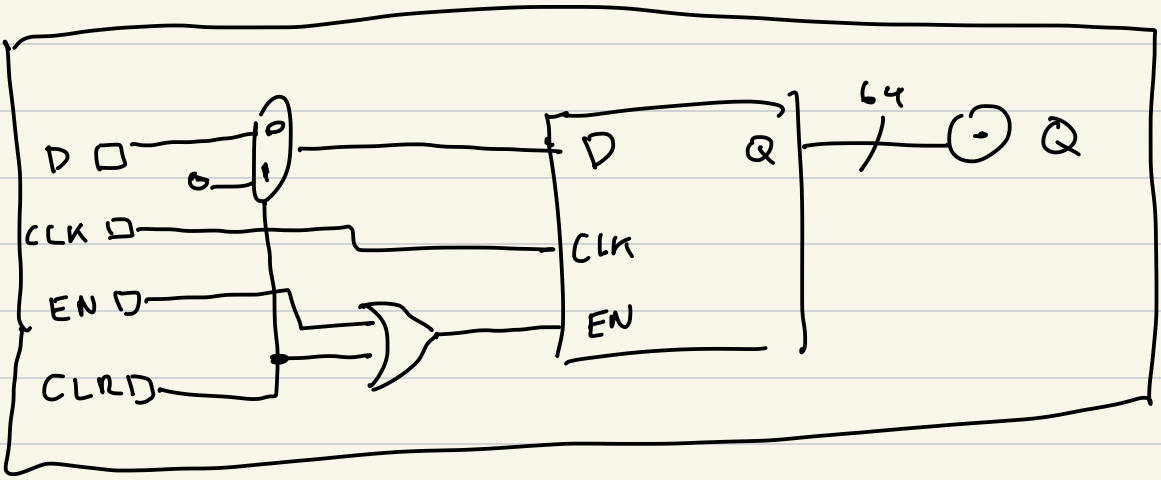
Register File

- 32 64-bit Registers: x0, x1, x2, ..., x31
- Read two register values on a clock cycle
- Write to one register on clock cycle
- x0 (zero) will always be zero (no updates)



RR read register #
RD read data
WR write register
WD write data
WE write enable

Adding CLR to the Digital Register



64 bit Reg with CLR

synchronous clear

Register File Implementation